Code.No: 07A5EC07 | R07 | SET-1

III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
COMPUTER ORGANIZATION
(COMMON TO ECE, EIE, ETM)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks
- - -

1.a) Explain clearly the terms – Computer Organization, Computer Architecture and Computer System Design.
b) Explain about the "sign magnitude" and "2's compliment" representations used for the fixed point numbers. Which among the above is most preferred and why? [8+8]

2.a) With the help of neat block diagrams explain the hardware that implements the following register transfer statement: $yT_2 : R2 \leftarrow R1,\quad R1 \leftarrow R2$.
b) What is a Register stack? Explain with relevant illustrations and examples. [8+8]

3.a) Write about the Control memory in detail.
b) Compare and contrast hardwired control and micro-programmed control. Is it possible to have a hardwired control associated with a control memory? [8+8]

4.a) Perform the arithmetic operations given below with binary and negative numbers in signed-2's complement representation. Use seven bits to accommodate each number together with its sign.
i) (-53) + (-80) ii) (-53) - (+80)
b) Explain the decimal division algorithm flowchart with a suitable example. [8+8]

5.a) A digital computer has a memory unit of 64K x 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words.
i) How many bits are there in the TAG, INDEX, BLOCK and WORD fields of the address format?
ii) How many bits are there in each word of cache, and how are they divided into functions? Include a valid bit.
b) Explain how the associative memory page table is used for effective storage utilization. [8+8]

6.a) What is an Input-Output interface? Explain the isolated versus memory-mapped I/O.
b) Write about the character-oriented protocol for the purpose of serial communication. [8+8]

7.a) Explain the instruction pipeline in detail with an example.
b) What is Vector processing? Explain how vector processing is related to supercomputer. [8+8]

8.a) Define a multiprocessor. Explain clearly the characteristics of multiprocessors.
b) Write about cache coherence. [8+8]

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COMPUTER ORGANIZATION
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Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks
- - -

1.a) With a neat diagram explain the bus structure of the computer and its significance.
b) Show the given decimal number 8620 in i) BCD ii) excess-3 code iii) 2421 code iv) binary number. [8+8]

2. Explain about direct, indirect, register direct, register indirect, immediate, implicit, relative, index, and base address mode of addressing. Is there a necessity for many addressing modes? Is the instruction size influenced by the number of addressing modes which a processor supports? State whether the number of addressing modes will be more in RISC or CISC? [16]

3.a) Define the following:
i) Microoperation ii) Microinstruction iii) Microprogram iv) Microcode
b) Write about the design of a control unit. [8+8]

4.a) Draw and explain in detail the hardware implementation of the signed-magnitude addition and subtraction.
b) Explain the decimal multiplication algorithm with a suitable example. [8+8]

5.a) A block-set associative cache consists of a total of 64 blocks divided into 4-block sets. The main memory contains 4096 blocks, each consisting of 128 words.
i) How many bits are there in a main memory address?
ii) How many bits are there in each of the TAG, SET and WORD fields?
b) Explain how page replacement management is handled in a virtual memory system. [8+8]

6.a) What is a priority interrupt? Explain about the Daisy-chaining priority in detail.
b) Explain the bit-oriented protocol for the serial communication. [8+8]

7.a) With the help of the suitable example explain in detail about the RISC pipeline.
b) Define Vector processing. Explain the relationship of vector processing with superscalar processors. [8+8]

8.a) What is a multiprocessor? Differentiate between tightly coupled and loosely coupled multiprocessiors with examples.
b) Explain about the Interprocessor arbitration. [8+8]

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Code.No: 07A5EC07 | R07 | SET-3

III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
COMPUTER ORGANIZATION
(COMMON TO ECE, EIE, ETM)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks
- - -

1.a) Explain the following terms:
i) Clock rate ii) Instruction set iii) Processor clock iv) Pipelining
b) Derive the circuits for a 3-bit parity generator and 4-bit parity checker using an odd-parity bit. [8+8]

2.a) Represent the following conditional control statement by two register transfer statements and control functions:
$If\ (P=1)\ then\ (R1 \leftarrow R2)\ else\ if\ (Q=1)\ then\ (R1 \leftarrow R3)$
b) Write about the Memory stack with relevant illustrations and examples. [8+8]

3.a) With a neat diagram explain the following with respect to Address sequencing:
i) Conditional branching ii) Mapping of Instruction iii) Subroutines.
b) Explain about the Microinstruction format with an example. [8+8]

4.a) Explain the algorithm of the hardware for addition and subtraction operations.
b) Explain the binary numbers multiplication process using Booth's algorithm in a step-by-step manner with a suitable example. Assume 5-bit registers that hold signed numbers. [8+8]

5.a) A block-set associative cache consists of a total of 64 blocks divided into 4-block sets. The main memory contains 4096 blocks, each consisting of 128 words.
i) How many bits are there in a main memory address?
ii) How many bits are there in each of the TAG, SET and word fields?
b) Write about the hardware for Memory management. [8+8]

6.a) Differentiate between the following:
i) I/O versus Memory bus
ii) Isolated versus Memory-mapped I/O
b) Write about Input-Output processor (IOP). [8+8]

7.a) With the help of the suitable example explain in detail about the Arithmetic pipeline.
b) Explain what is meant by memory interleaving with respect to vector processing. [8+8]

8.a) Write about multistage switching network with suitable illustrations.
b) Explain the various dynamic arbitration algorithms used for the interprocessor arbitration. [8+8]

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Code.No: 07A5EC07 | R07 | SET-4

III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
COMPUTER ORGANIZATION
(COMMON TO ECE, EIE, ETM)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks
- - -

1.a) With a neat diagram and example of an operation, explain clearly how the basic operations are performed in a computer in terms of the processor and memory.
b) Derive the circuits for a 3-bit parity generator and 4-bit parity checker using an even-parity bit. [8+8]

2.a) Define a micro operation. Explain clearly at least four logic micro operations with examples.
b) With an example clearly explain the following address modes:
i) Direct ii) Indirect iii) Relative iv) Indexed. [8+8]

3.a) Explain about the address sequencing with neat illustration.
b) Explain the difference between a microprocessor and a microprogram? Is it possible to design a microprocessor without a microprogram? Are all microprogrammed computers also microprocessors? [8+8]

4.a) Explain the Booth's algorithm for the binary numbers multiplication process using a suitable example. Assume 5-bit registers that hold signed numbers.
b) Explain the decimal division algorithm with a suitable example. [8+8]

5.a) A digital computer has a memory unit of 64K x 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words.
i) How many bits are there in the TAG, INDEX, BLOCK and WORD fields of the address format?
ii) How many bits are there in each word of cache, and how are they divided into functions? Include a valid bit.
b) Write about the Virtual memory. [8+8]

6. Explain the following:
a) Direct Memory Access.
b) Isolated versus memory-mapped I/O
c) CPU –IOP communication. [6+5+5]

7.a) What is parallel processing? Explain the significance of parallel processing. List the Flynn's classification of computers.
b) Define Array processors. Explain how are attached array processors different from SIMD array processors? [8+8]

8.a) What are Interconnection structures? Explain the scheme Crossbar switch in detail.
b) Write about the Interprocessor arbitration. [8+8]

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